

ADC Measurement

Outline

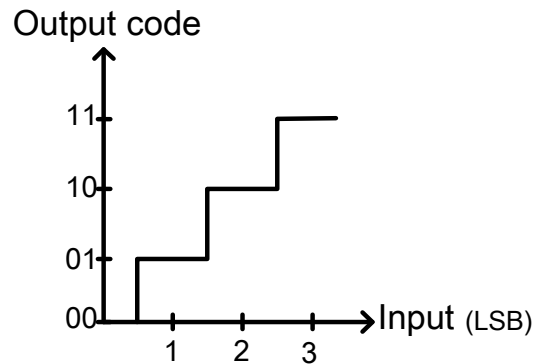
- Introduction of ADC
- Static testing
- Dynamic testing
- Measurement example
- Reference

Introduction of ADC

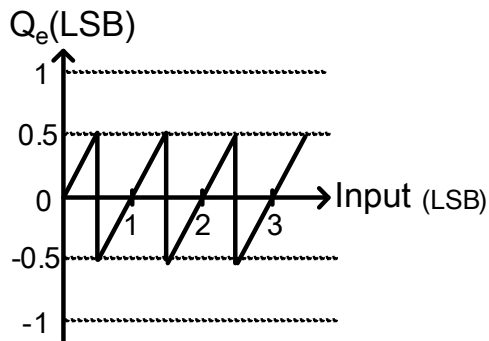
- Conversion of signal from analog to digital

- Ideal 2-bit ADC

- ◆ Input-output transfer curve

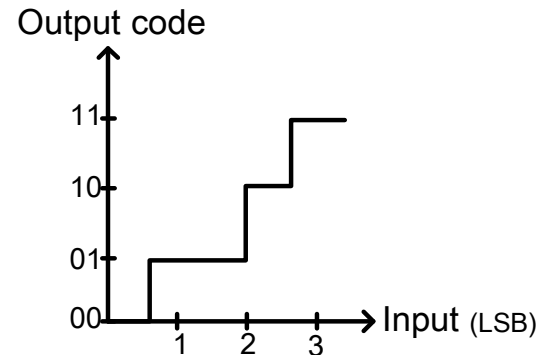


- ◆ Quantization error

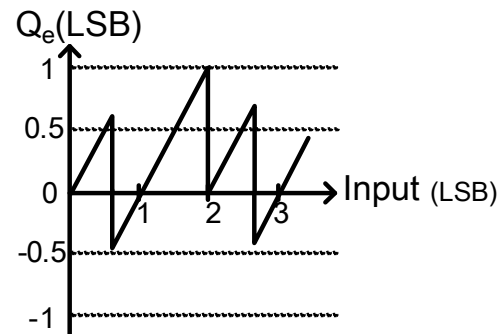


- Non-ideal 2-bit ADC

- ◆ Input-output transfer curve



- ◆ Quantization error



Outline

- Introduction of ADC
- Static testing
 - ◆ Static errors
 - ◆ Histogram testing
 - Ramp signal
 - Sinusoidal signal
 - A_{\sin} Fitting Methods
 - Summary of A_{\sin} Fitting Methods
 - Normalization of transitions
 - Consideration of offset voltage
 - Illustration of relationship between threshold voltage and output code
 - The Influence of input amplitude to histogram
 - Verification of MATLAB code for static testing
 - ◆ Aperture Uncertainty Measurement
 - ◆ Limitation of number of sampling points

Outline(Cont.)

- Dynamic testing
- Measurement example
- Reference

Static Testing

- Introduction of static errors with a 3-bit ADC

- ◆ Offset

- ◆ Gain error

- ◆ Differential nonlinearity (DNL)

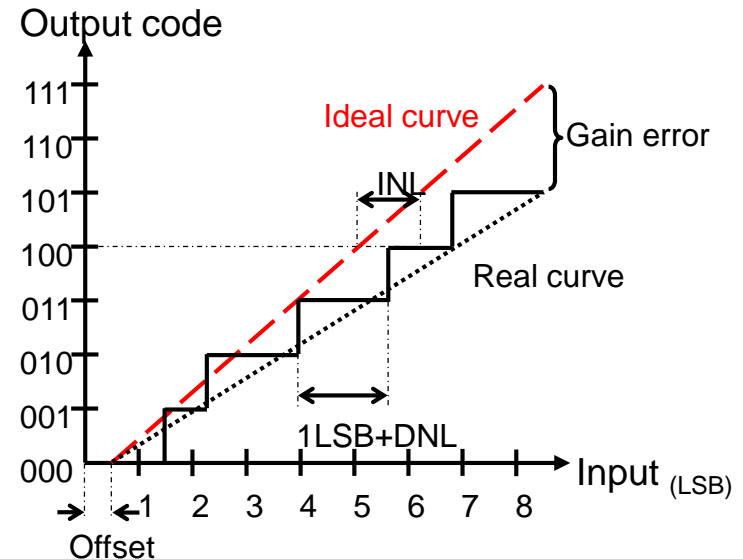
- The difference between an actual step width and the ideal value of 1 LSB

- $$DNL(k) = \frac{\text{code width}(k) - 1\text{LSB}}{1\text{LSB}}, \quad k: \text{output code}$$

- ◆ Integral nonlinearity (INL)

- Deviation of code transition from its ideal location

- $$INL(k) = \sum_{i=1}^k DNL(i)$$



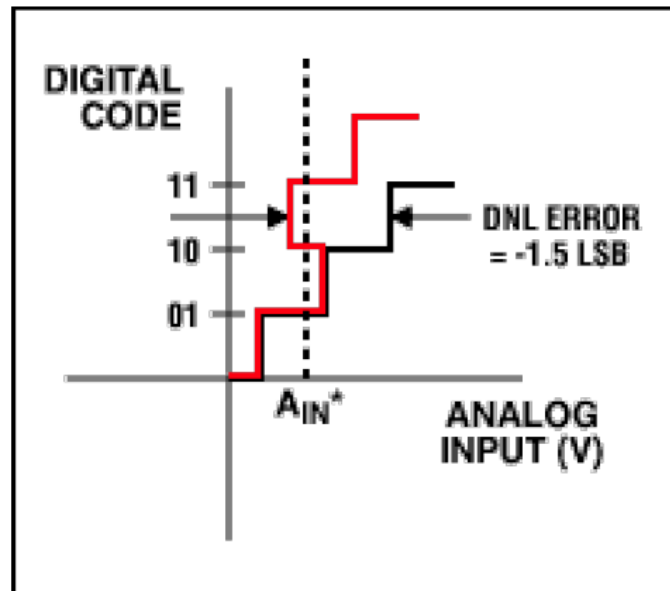
DNL < -1?

- DNL is defined as:

$$DNL(k) = \frac{\text{code width}(k) - 1\text{LSB}}{1\text{LSB}}$$

→ DNL < -1 if and only if code width < 0

- Transfer curve of DNL < -1 case[8]

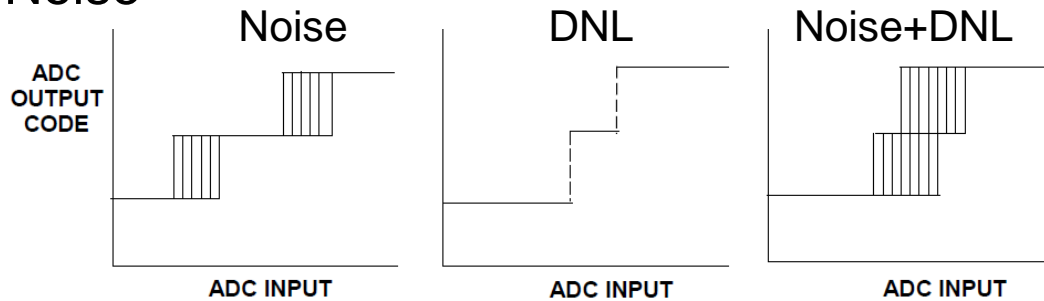


At A_{IN^*} the digital code can be one of three possible values. When the input voltage is swept, Code 10 will be missing.

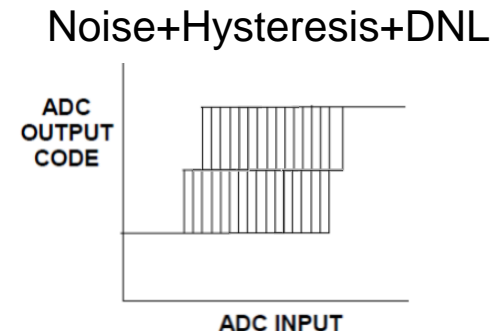
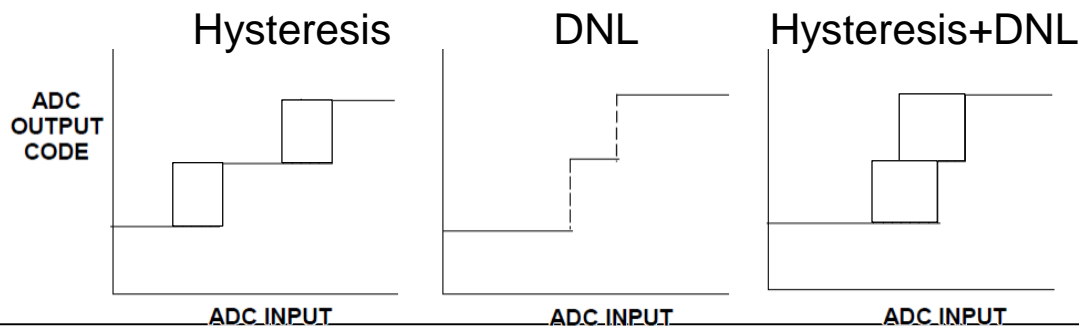
Measurement of DNL <-1

- Measurement detecting transition points[9]
 - ◆ LED display test
 - ◆ Integrating servo-loop test
 - ◆ Computer controlled servo-loop test
- More than one output possibility with same input

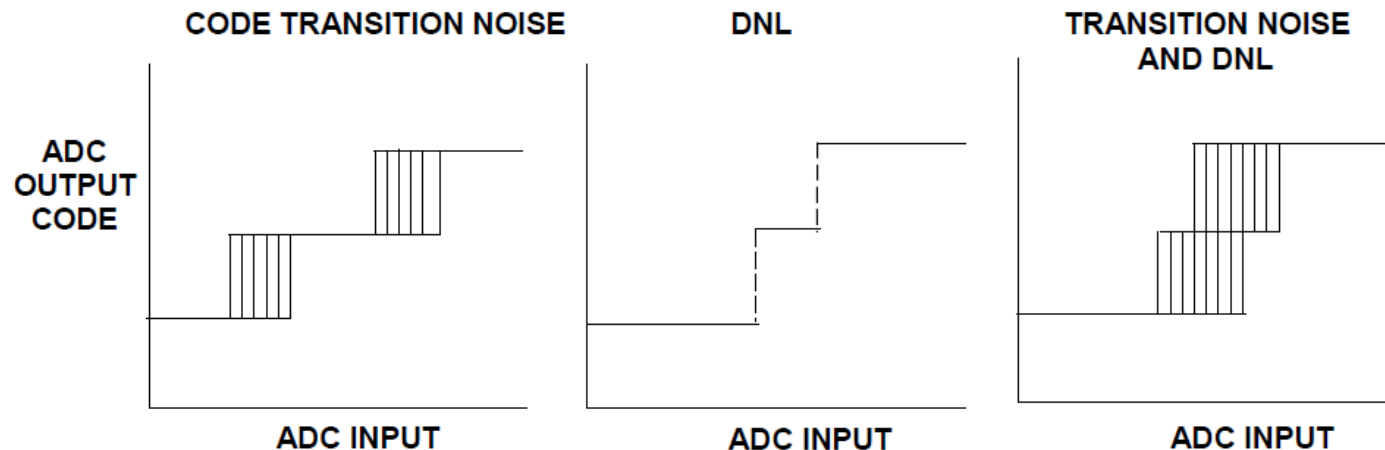
◆ Noise



◆ Hysteresis



Combined Effect of Code transition Noise and DNL



- "No missing codes" can be defined as a combination of transition noise and DNL which guarantees some level (perhaps 0.2 LSB) of noise-free code for all codes.
- Within large noise, the manufacturer must define "noise levels" and "resolution" in some other way. Which method is used is less important, but the data sheet should contain a clear definition of the method used and the performance to be expected[10]

Histogram Testing

- Features

- ◆ Averaging effect of noise and hysteresis
 - Suitable for very high resolution or wide bandwidth sampling ADCs
- ◆ Monotonic assumption
 - Not accurate while testing non-monotonic ADCs

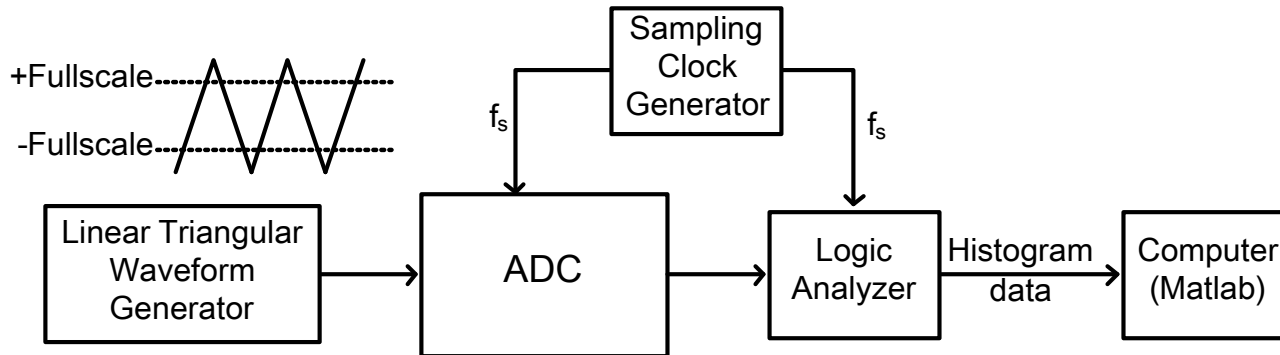
- Testing steps

- ◆ Applying input signal (e.g. ramp wave, sinusoidal wave) with known probability density function (PDF)
- ◆ Measurement of output PDF
- ◆ Using histogram to calculate DNL and INL

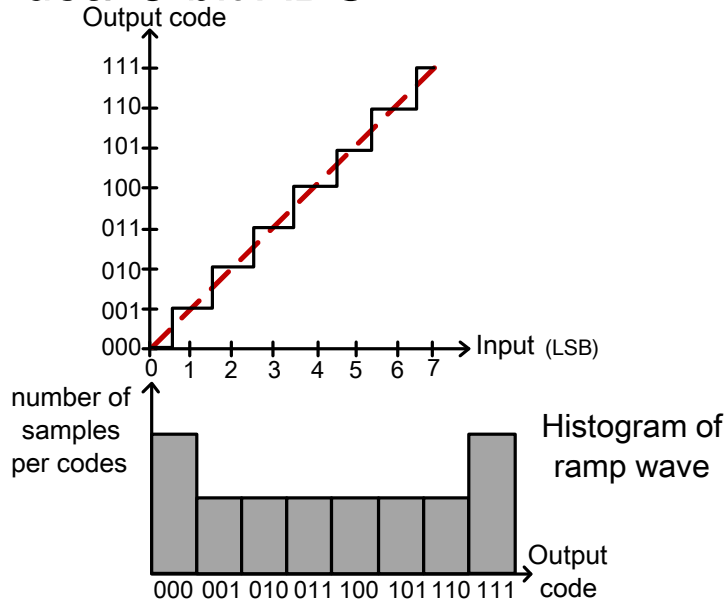
➔ Widely used in modern static testing

Histogram Testing with Ramp Signal

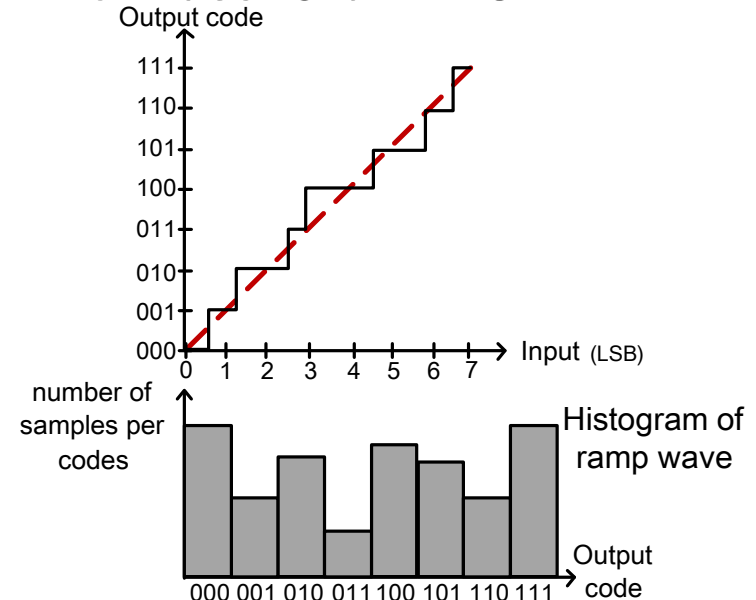
- A linear triangular waveform which slightly exceeds both ends of the ADC range is usually used for testing



● Ideal 3-bit ADC



● Non-ideal 3-bit ADC



Histogram Testing with Ramp Signal (Cont.)

- DNL calculation

- ◆ Removing the histogram results of min. and max. output codes

- ◆ Normalizing histogram results to mean value

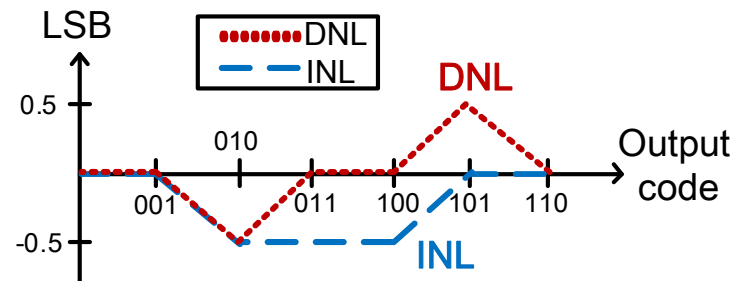
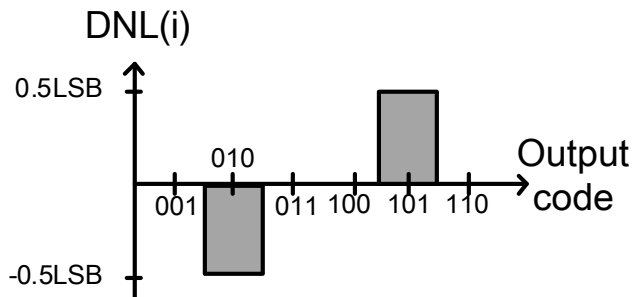
$$\Rightarrow h_{normal}(i) = \frac{h(i)}{mean(h(i))}$$

- ◆ Subtracting 1 from the normalized histogram to get DNL(i)

$$\Rightarrow DNL(i) = h_{normal}(i) - 1$$

- INL calculation

The formula of i-th INL is $INL(i) = \sum_{k=1}^{i-1} DNL(k)$ (end-point)



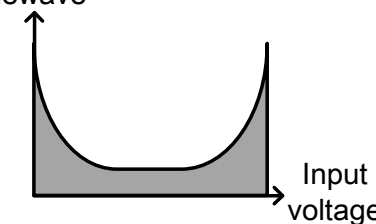
- Disadvantage of histogram testing with ramp signal

Hard to filter the out-of-band noise because triangle wave is composed by many different frequencies

$$\Rightarrow \text{Ideal triangular wave: } x_{triangle}(t) = \frac{8}{\pi^2} (\sin(\omega t) - \frac{1}{9} \sin(3\omega t) + \frac{1}{25} \sin(5\omega t) + \dots)$$

Histogram Testing with Sinusoidal Signal

- The probability density of sinusoidal signal
 - ◆ A_{\sin} is the amplitude of sine wave, V_a and V_b are any voltage in the interval of $(-A_{\sin}, A_{\sin})$
 - ◆ $P(V_a, V_b) = \frac{1}{\pi} \{ \sin^{-1}[\frac{V_b}{A_{\sin}}] - \sin^{-1}[\frac{V_a}{A_{\sin}}] \}$, which $V_b > V_a$...eq.(1) Probability density of sinewave
 - ◆ Assume $V_b - V_a = 1\text{LSB}$, converting continuous probability $P(V_a, V_b)$ to discrete probability $P(i)$



$$\Rightarrow P(i) = \frac{1}{\pi} \{ \sin^{-1}[\frac{V_{\text{LSB}} \cdot (i - 2^{N-1})}{A_{\sin}}] - \sin^{-1}[\frac{V_{\text{LSB}} \cdot (i - 1 - 2^{N-1})}{A_{\sin}}] \} \dots \text{eq.}(2)$$

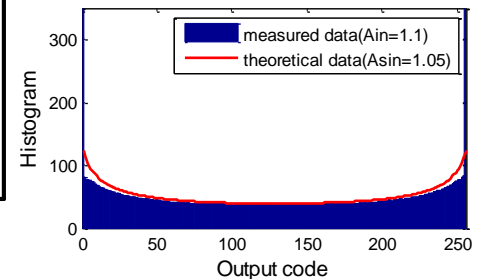
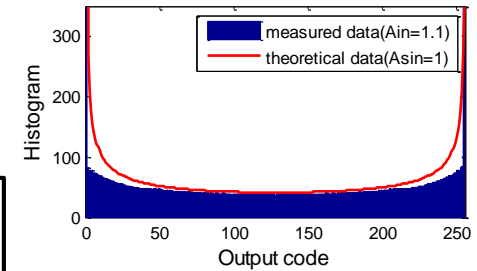
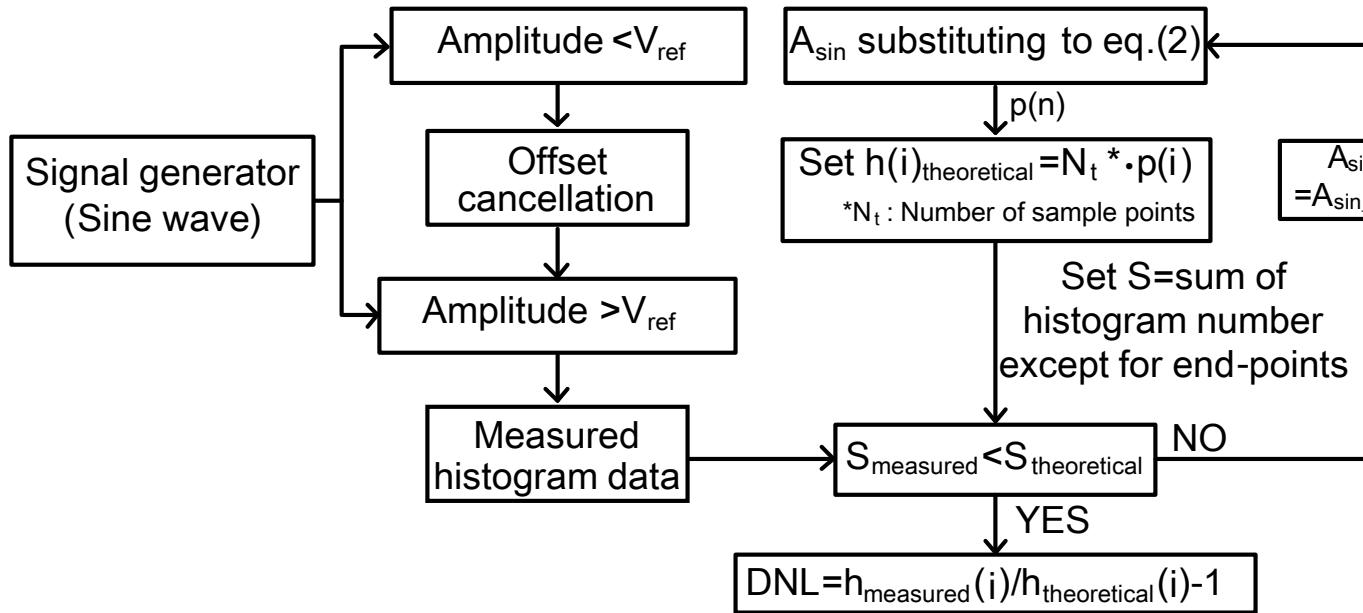
- Let $h(i)$ be the histogram result of n -th output code

DNL can be calculated by $\frac{h(i)}{N_t} - 1 \dots \text{eq.}(3)$ $\left\{ \begin{array}{l} N_t : \text{number of sample points} \\ P_{\text{ideal}}(i) : \text{PDF of ideal sine wave input} \end{array} \right.$

- ◆ However, this formula is unfeasible to get DNL because A_{\sin} must be known with great precision
- ◆ To overcome this problem, different methods are proposed by different companies

A_{sin} Fitting Methods

- Method-1 from Maxim[11]
 - ◆ We can't get real amplitude information A_{in} and only know the estimated amplitude information A_{sin}
 - ◆ Flow chart of method-1



Advantage	Accurate DNL information
Disadvantage	Exhausting analysis and iterative simulation

A_{sin} Fitting Methods (Cont.)

- Method-2 from ADI[10]

- ◆ Procedure of DNL calculation

- A_{sin} should be estimated to $\frac{V_{FS}}{\sin\left(\frac{N_t}{N_t + h(0) + h(2^N - 1)} \cdot \frac{\pi}{2}\right)} \dots \text{eq.(4)}$

- which $V_{FS} \approx$ full-scale voltage

- Estimated value of A_{sin} from eq.(4) is used in eq.(2)

- $\Rightarrow h(i)_{theoretical} = p(i) \cdot N_t$

- DNL could be calculated by eq.(3) $\Rightarrow DNL(i) = \frac{h(i)_{measured}}{h(i)_{theoretical}} - 1$

- ◆ MATLAB verification

$f_s=80\text{MHz}$ $f_{in}=9.82\text{MHz}$ $N_t=2^{14}; V_{ref}=2\text{V}$	A_{in}	A_{sin}
	2 V _{p-p}	2.0158 V _{p-p}
	3 V _{p-p}	3.0238 V _{p-p}

- ◆

Advantage	A _{sin} is estimated directly
Disadvantage	Not accurate enough in high-resolution ADC

Summary of A_{\sin} Fitting Methods

- In method-1: iteration times \propto accuracy
- In method-2: accuracy of DNL information is not good enough in high-resolution ADC
- Except A_{\sin} fitting methods, we could get accurate DNL information quickly by abandoning both ends codes* information based on [1]
 - ◆ To get DNL information, recovering the real transition level from normalized transition level would be used
 - ◆ The details of this method will be introduced in the next pages

* Both ends codes is acquired from the measured codes

Normalization of Transitions

- Before normalizing, $P(i)$ is replaced with $\frac{h(i)}{N_t}$ in eq.(2) to calculate threshold voltage, $V(i)$

$$P(i) = \frac{1}{\pi} \left\{ \sin^{-1} \left[\frac{V_{LSB} \cdot (i - 2^{N-1})}{A_{\sin}} \right] - \sin^{-1} \left[\frac{V_{LSB} \cdot (i - 1 - 2^{N-1})}{A_{\sin}} \right] \right\}$$

$$\Rightarrow \frac{h(i)}{N_t} = \frac{1}{\pi} \left\{ \sin^{-1} \left[\frac{V(i)}{A_{\sin}} \right] - \sin^{-1} \left[\frac{V(i-1)}{A_{\sin}} \right] \right\}$$

$$\Rightarrow V(i) = V(i-1) \cos\left(\frac{\pi \cdot h(i)}{N_t}\right) + \sin\left(\frac{\pi \cdot h(i)}{N_t}\right) \sqrt{A_{\sin}^2 - V^2(i-1)}$$

Set boundary condition $V(0) = -A_{\sin}$

$$\Rightarrow V(i) = -A_{\sin} \cos\left(\frac{\pi \cdot \sum h(i)}{N_t}\right)$$

- $V(i)$ can be normalized to A_{\sin}

$$\Rightarrow V(i) = -\cos\left(\frac{\pi \sum h(i)}{N_t}\right)$$

- ◆ The full range of transitions is $(-1, +1)$
- ◆ Before recovering the real transition, some assumptions about initial condition are necessary

Consideration of Offset Voltage

- Offset could be calculated by histogram
 - ◆ If $V_{\text{offset}}=0\text{V}$, the number of codes above zero (N_p) equals the number of codes below zero (N_n)
 - ◆ Let p_p be the probability of positive sampled voltage which in the range of $(0, A_{\text{sin}}+V_{\text{offset}})$, and p_n is the probability of negative sampled voltage which in the range of $(-A_{\text{sin}}+V_{\text{offset}}, 0)$

$$\Rightarrow V_{\text{offset}} = A_{\text{sin}} \sin\left(\frac{\pi}{2} \cdot (p_p - p_n)\right) = A_{\text{sin}} \sin\left(\frac{\pi}{2} \cdot \left(\frac{N_p - N_n}{N_t}\right)\right)$$

- Correction of transitions with offset error

- ◆ $V(i) = -A_{\text{sin}} \cos\left(\frac{\pi \cdot \sum h(i)}{N_t}\right) + A_{\text{sin}} \sin\left(\frac{\pi}{2} \cdot (p_p - p_n)\right)$

- ◆ $V(i)$ could also be normalized to A_{sin}

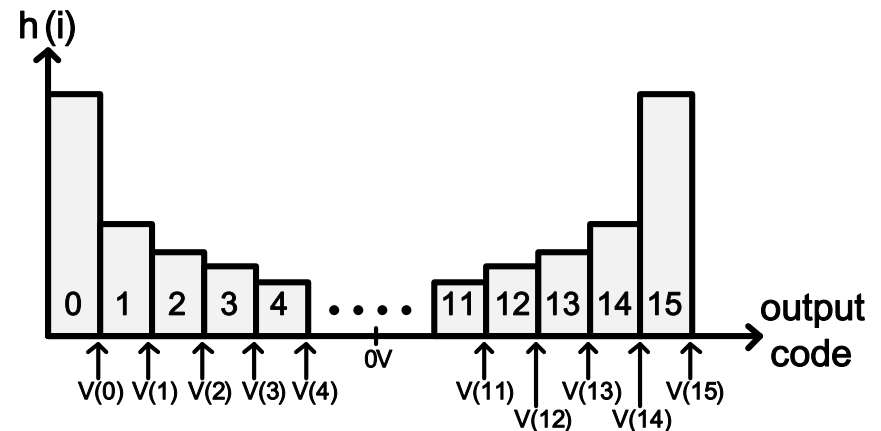
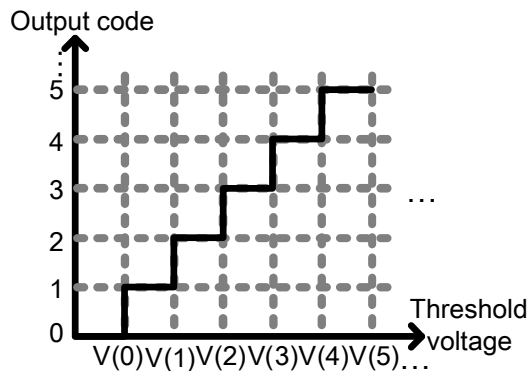
$$\Rightarrow V(i) = -\cos\left(\frac{\pi \cdot \sum h(i)}{N_t}\right) + \sin\left(\frac{\pi}{2} \cdot \left(\frac{N_p - N_n}{N_t}\right)\right)$$

Illustration of Relationship between Threshold Voltage and Output Code

- Presentation of threshold voltage $V(i)$ with a 4-bit example

- ◆ $V(i) = -\cos\left(\frac{\pi h(i)}{N_t}\right)$

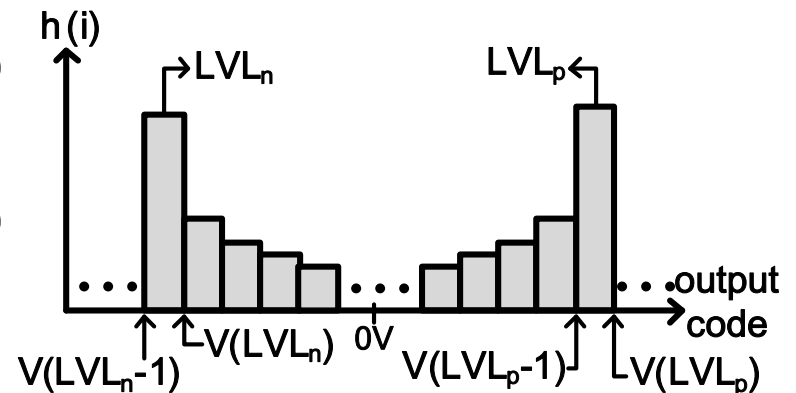
- ◆ Input-output transfer curve



- Definition of LVL_n and LVL_p

- ◆ LVL_n : the output level with max. $h(i)$ value in negative voltage

- ◆ LVL_p : the output level with max. $h(i)$ value in positive voltage

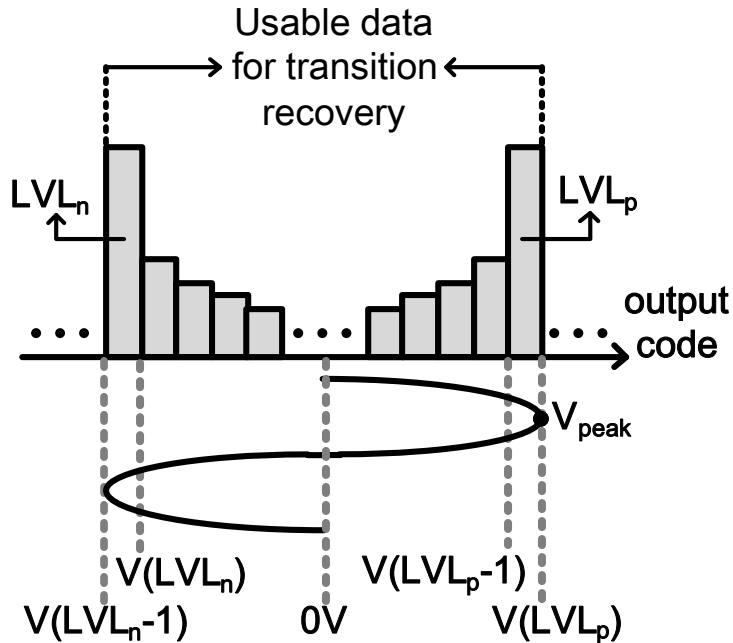


The Influence of Input Amplitude to Histogram

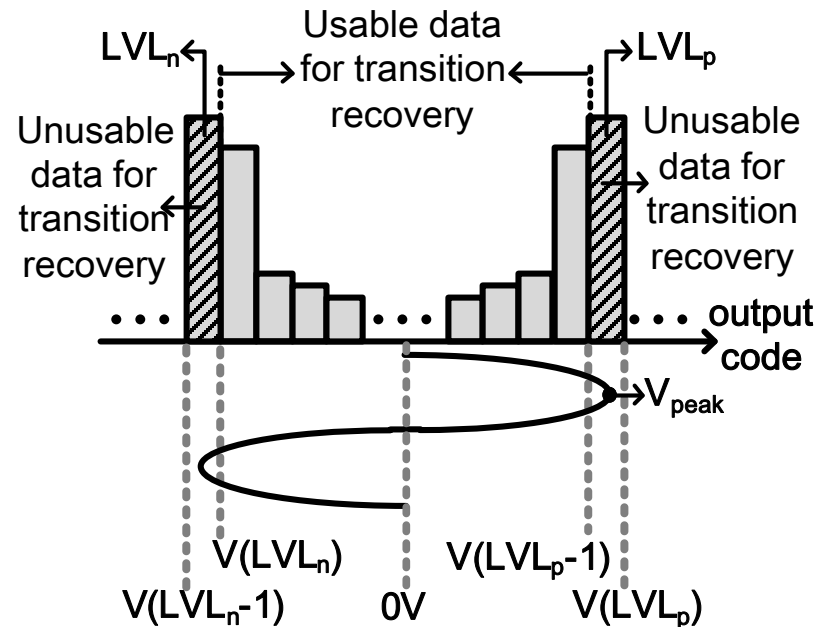
- There are three kinds of conditions under test

- ◆ V_{peak} is equals to $V(LVL_p)$

- ◆ V_{peak} is slightly smaller than $V(LVL_p)$



Usable range:
 $V(LVL_{n-1}) \sim V(LVL_p)$

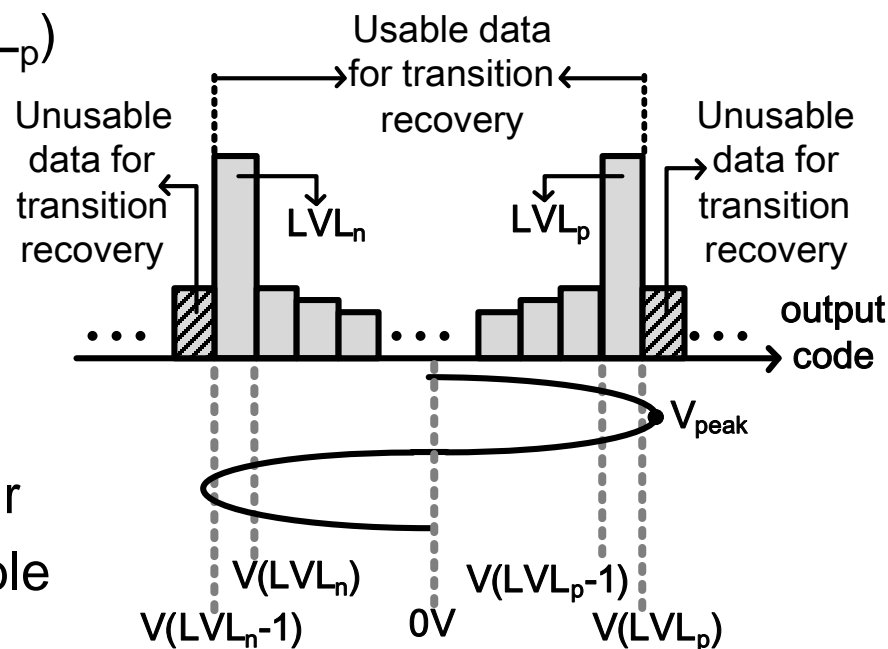


Usable range:
 $V(LVL_n) \sim V(LVL_{p-1})$

The Influence of Input Amplitude to Histogram (Cont.)

- ◆ V_{peak} is slightly larger than $V(\text{LVL}_p)$

Usable range:
 $V(\text{LVL}_n-1) \sim V(\text{LVL}_p)$



- Because the above conditions occur randomly, we need to take the usable data in the range from $V(\text{LVL}_n)$ to $V(\text{LVL}_p-1)$ in order to recover the correct transitions
- DNL of unused codes are set to zero
 - ◆ $\text{DNL}(0) = \text{DNL}(1) = \dots = \text{DNL}(\text{LVL}_n) = 0$
 - ◆ $\text{DNL}(\text{LVL}_p) = \text{DNL}(\text{LVL}_p+1) = \dots = \text{DNL}(2^{\text{bit}}-1) = 0$

Calculation of DNL and INL

- Recovery of the real transitions from normalized transitions

- ◆ Find the LVL_n and LVL_p

- ◆ Create the transitions normalized to A_{\sin}

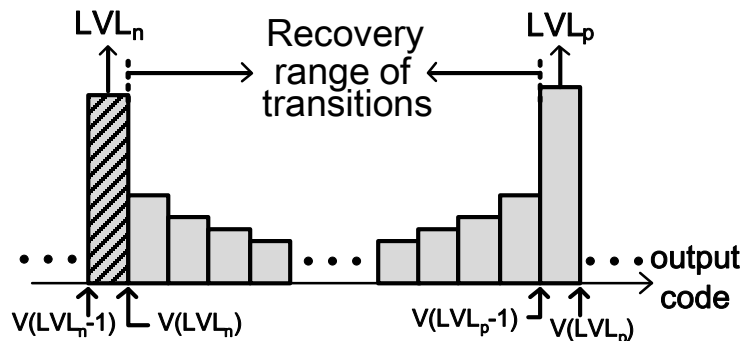
$$V(i) = -\cos\left(\frac{\pi \cdot \sum h(i)}{N_t}\right) + V_{offset} = -\cos\left(\frac{\pi \cdot \sum h(i)}{N_t}\right) + \sin\left(\frac{\pi}{2} \cdot \left(\frac{N_p - N_n}{N_t}\right)\right)$$

- ◆ Recover the normalized transitions to real voltage

$$V_{real}(i) = \frac{\text{Difference between } V(LVL_p - 1) \text{ and } V(LVL_n) \text{ for real transitions}}{\text{Difference between } V(LVL_p - 1) \text{ and } V(LVL_n) \text{ for normalized transitions}} \cdot V(i)$$

$$= \frac{(LVL_p - LVL_n - 2) \cdot V_{LSB}}{V(LVL_p - 1) - V(LVL_n)} \cdot V(i)$$

➔ The transitions from $V(LVL_n)$ to $V(LVL_p - 1)$ are recovered



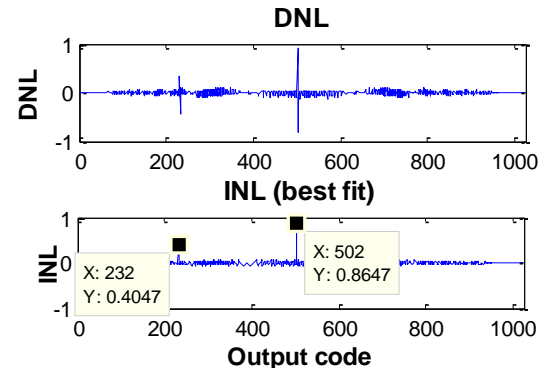
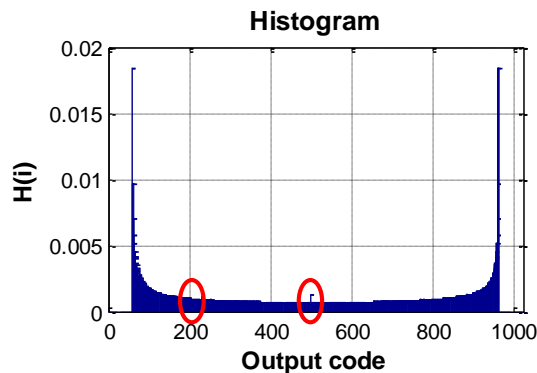
Calculation of DNL and INL (Cont.)

- DNL and INL can be calculated with recovered transitions
 - ◆ $DNL(i) = V_{real}(i) - V_{real}(i-1)$, which $i = (LVL_n + 1) \sim (LVL_p - 1)$
 - ◆ Based on previous assumption, DNL of unused code are set to zero
 - $DNL(0) = DNL(1) = \dots = DNL(LVL_n) = 0$
 - $DNL(LVL_p) = DNL(LVL_p + 1) = \dots = DNL(2^{bit} - 1) = 0$
 - ◆ $INL(i) = \sum_{k=0}^i DNL(k)$, which $i = 0 \sim (2^{bit} - 1)$

Verification of MATLAB Code for Static Testing

- Artificial non-ideal ADC with given DNL

- ◆ Set $DNL(500)=0.8$, $DNL(501)=-0.8$, $DNL(230)=0.4$, $DNL(231)=-0.4$



10bits
 $V_{ref}=1.7V$
 $A_{input}=1.5V$
 $N_t=2^{16}$

➤ Comparison between different conditions

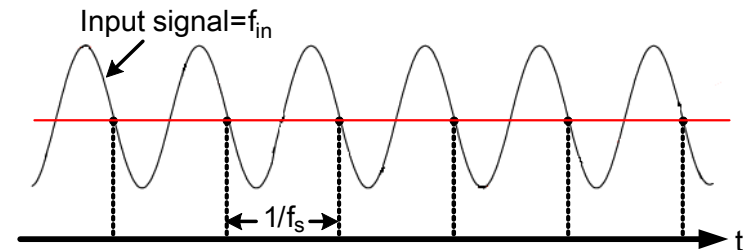
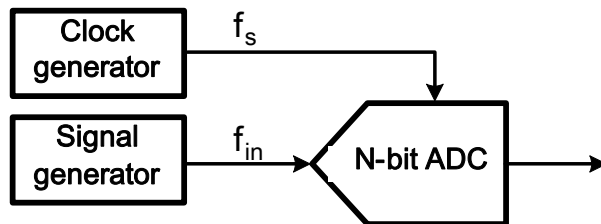
	DNL(500)	DNL(501)	DNL(230)	DNL(231)
All $DNL(i)=0$	0	0	0	0
Verification results	0.04	0.04	-0.051	-0.049
Given $DNL(i)$	0.8	-0.8	0.4	-0.4
Verification results	0.905	-0.83	0.3557	-0.457

- ◆ This method is verified in the artificial ADC

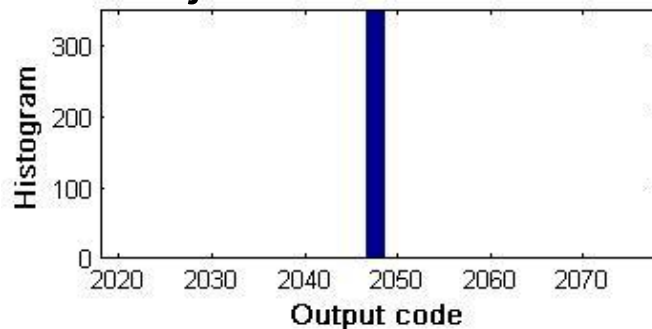
Aperture Uncertainty Measurement

- Locked histogram testing [13]

- ◆ Set f_{in} equals to f_s

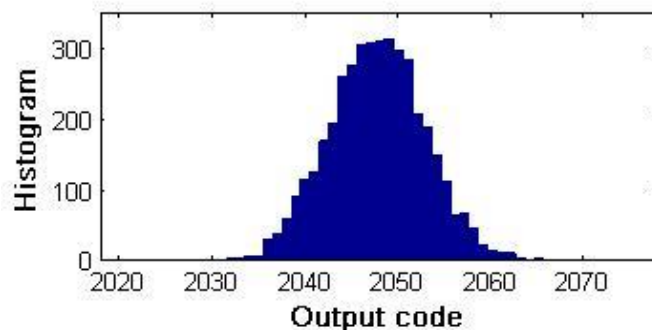


- ◆ Without jitter effect → Hit the same code



12-bit ADC
 $f_{in}=f_s=20\text{MHz}$
 $\sigma_{\text{Jitter}}=0\text{ps}$

- ◆ With jitter effect → Get σ_{Jitter} from histogram



12-bit ADC
 $f_{in}=f_s=20\text{MHz}$
 $\sigma_{\text{Jitter}}=20\text{ps}$

Limitation of Number of Sampling Points

- Number of sample points (N_t)

- ◆
$$N_t \geq \frac{Z_{\alpha/2}^2 \cdot \pi \cdot 2^{N-1}}{\beta^2}$$
 - N : Number of bit
 - β : DNL resolution in LSB
 - $Z_{\alpha/2}$: Number of standard deviations from the mean values

- ◆ Calculated DNL lies in range $(\mu - Z_{\alpha/2} \cdot \sigma, \mu + Z_{\alpha/2} \cdot \sigma)$ with $100(1-\alpha)$ percent probability, where μ is expected value, σ is standard deviation and α is chosen desired confidence level

- ◆ Standard normal distribution table for the given α

α	Confidence(1- α)	$Z_{\alpha/2}$
0.1	90%	1.64
0.05	95%	1.96
0.02	98%	2.33
0.01	99%	2.58

- ◆ Example of a 10-bit ADC with 0.01LSB precision and 99% confidence

$$N_t \geq \frac{2.58^2 \cdot \pi \cdot 2^{10-1}}{0.01^2} = 107067890 \approx 2^{26}$$

Outline

- Introduction of ADC
- Static testing
- Dynamic testing
 - ◆ Coherent sampling
 - ◆ Introduction of window function
 - ◆ Performance metrics of dynamic testing
 - ◆ ENOB Calculation
- Measurement example
- Reference

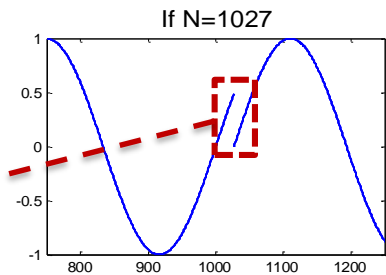
Coherent Sampling

- Relationship between input frequency, sample frequency, number of cycles and number of samples

$$\Rightarrow \frac{f_{in}}{f_s} = \frac{N_{cycles}}{M_{samples}} \begin{cases} f_{in} : \text{input frequency}, N_{cycles} : \text{number of cycles} \\ f_s : \text{sample frequency}, M_{samples} : \text{number of samples} \end{cases}$$

◆ Non-coherent sampling

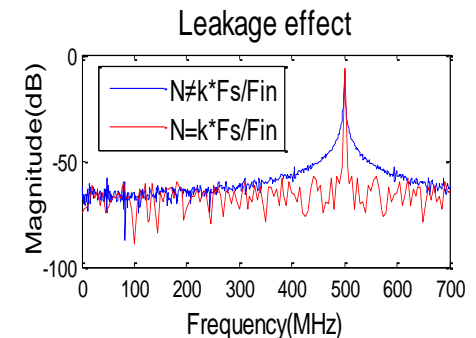
- N_{cycles} is non-integral
 - In frequency domain → leakage effect
 - In time domain → discontinuity



- N_{cycles} is integral but N_{cycles} and $M_{samples}$ are not co-prime
 - Discontinuity elimination
 - Periodicity of quantization error

◆ Coherent sampling

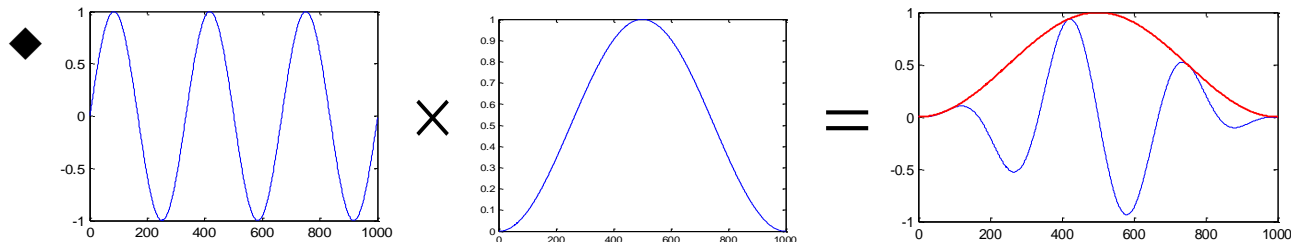
- N_{cycles} is prime number
 - Quantization error is not periodic



- Another method of solving discontinuity is applying window

Introduction of Window Function

- Applying window to signal

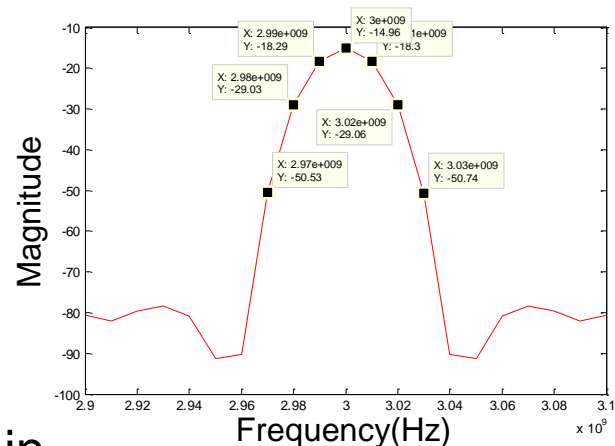
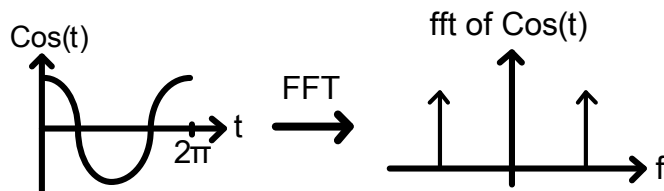


- Blackman-Harris window (Minimum-4-terms window)

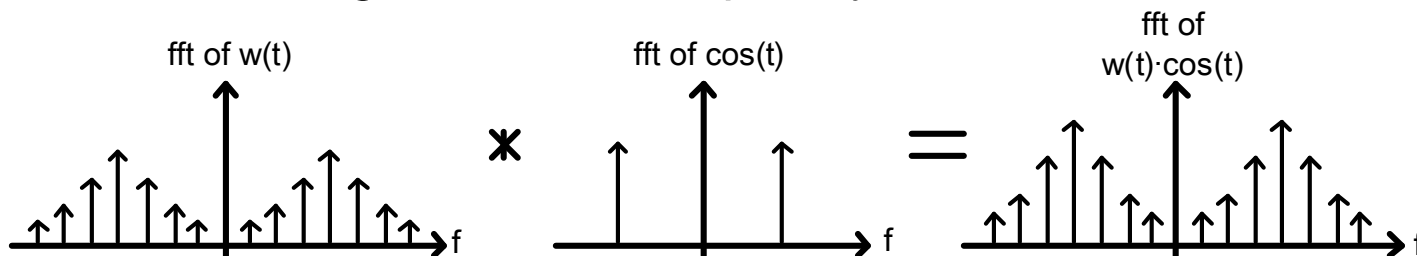
◆ $w[n] = a_0 - a_1 \cos\left(\frac{2\pi n}{N-1}\right) + a_2 \cos\left(\frac{4\pi n}{N-1}\right) - a_3 \cos\left(\frac{6\pi n}{N-1}\right)$

$a_0 = 0.3588, a_1 = 0.4883, a_2 = 0.1413, a_3 = 0.0117$

◆ $\cos(x) = \frac{e^{jx} + e^{-jx}}{2}$



- ◆ Effect of adding window in frequency domain



Performance Metrics of Dynamic Testing

- SNR(Signal-to-Noise Ratio)

$$SNR = 10 \cdot \log_{10} \left(\frac{P_{signal}}{P_{noise}} \right)$$

- SNDR(Signal-to-Noise and Distortion Ratio)

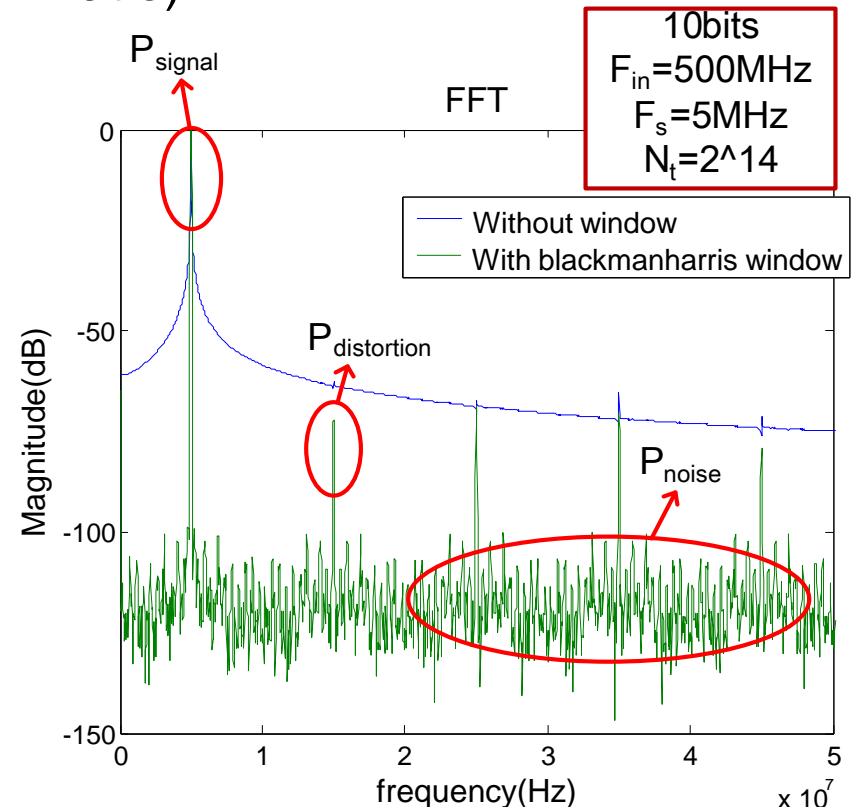
$$SNDR = 10 \cdot \log_{10} \left(\frac{P_{signal}}{P_{noise} + P_{distortion}} \right)$$

- Total Harmonic Distortion + Noise

$$THD + N = \left(\frac{P_{noise} + P_{distortion}}{P_{signal}} \right) \times 100\%$$

- Spurious-Free Dynamic Range

$$SFDR = 10 \cdot \log_{10} \left(\frac{P_{signal}}{P_{max-tone}} \right)$$

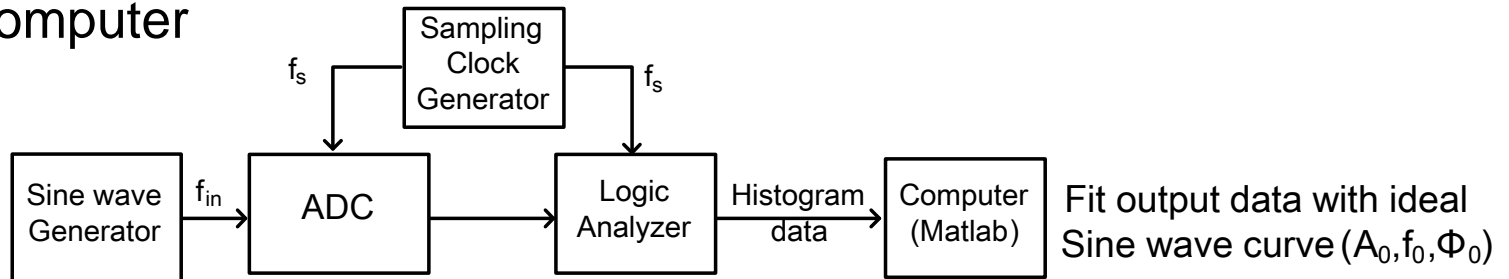


ENOB Calculation

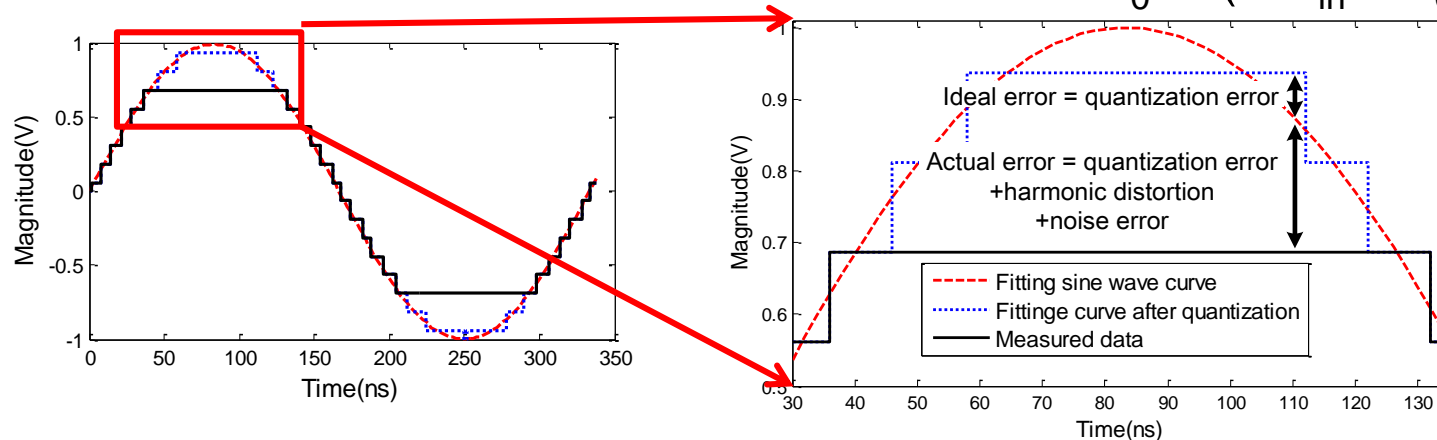
- Two methods for ENOB calculation

- ◆ Sine wave curve fitting [10], [12]

- Measured data are acquired by logic analyzer and processed by computer



- Fit the measured data with the sine wave $A_0 \sin(2\pi f_{in} t + \Phi_0) + V_{os}$



- $ENOB = N - \log_2 \left(\frac{\text{actual rms error}}{\text{ideal rms error}} \right)$; ideal rms error = $\frac{V_{LSB}}{\sqrt{12}}$

ENOB Calculation(Cont.)

- ◆ Relationship between SNDR and ENOB [1]

- With full-scale input

$$\text{ENOB} = \frac{\text{SNDR} - 1.76}{6.02} \text{ (bit)}$$

- Without full-scale input

$$\text{ENOB} = \frac{\text{SNDR} - 1.76 + \Delta x}{6.02} \text{ (bit)}$$

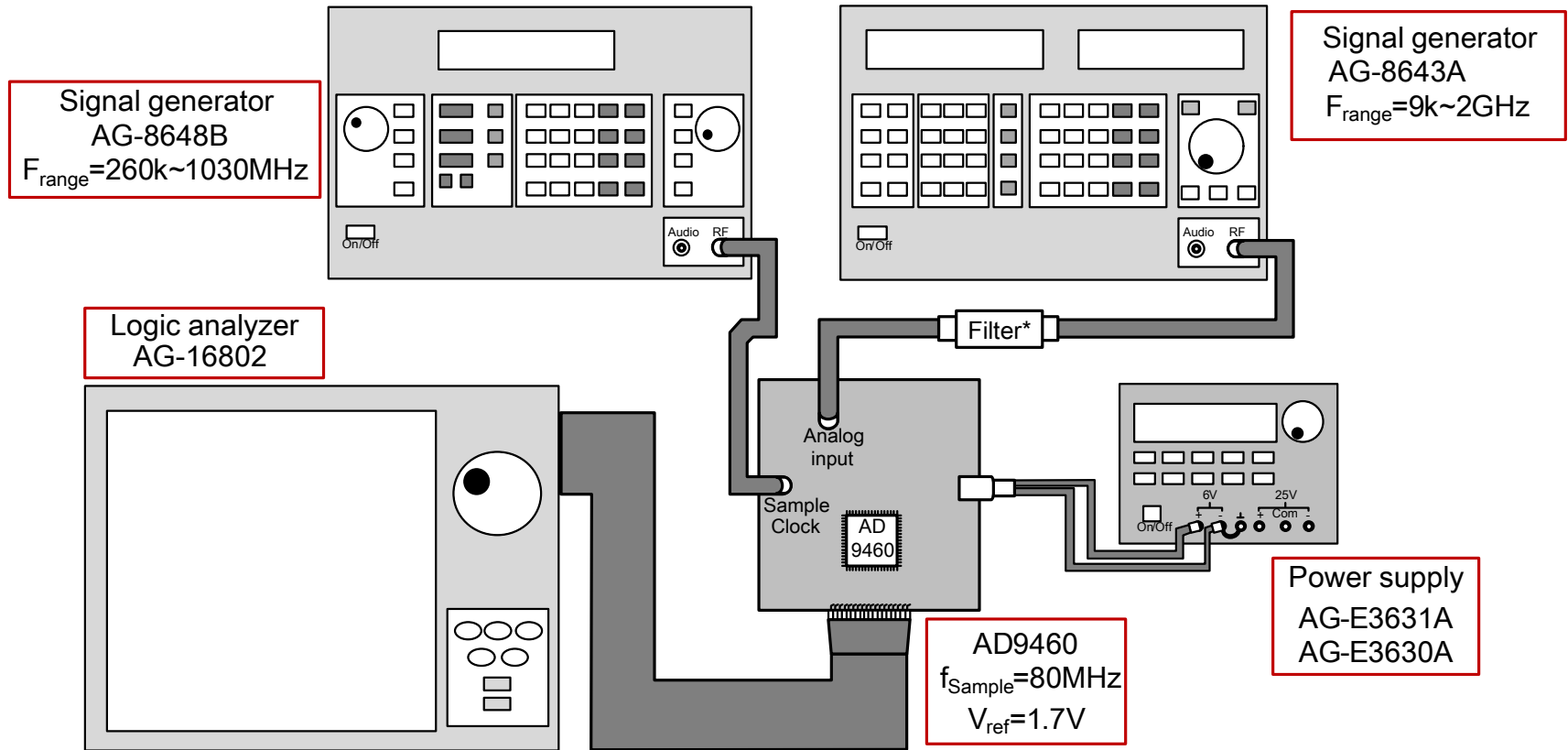
$\Delta x \approx$ Level of signal below full - scale(dB)

Outline

- Introduction of ADC
- Static testing
- Dynamic testing
- Measurement example
 - ◆ Setup of ADC measurement
 - ◆ Static testing
 - Relationship between DNL and number of sample points
 - Mismatch between A_{in} and A_{sin}
 - Comparison of static performance
- Reference

ADC Measurement Setup

- ADC measurement setup



- *Filter

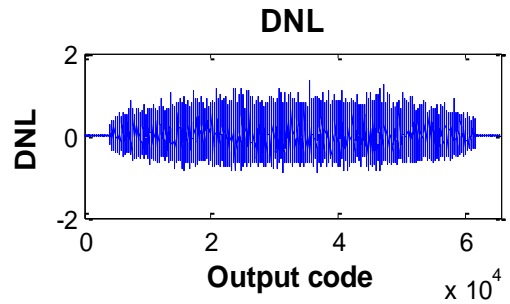
- ◆ Low pass filter: TTE-LC7-10M-LPF
- ◆ Band pass filter: K&L-5M-BPF

Relationship between DNL and Number of Sample Point

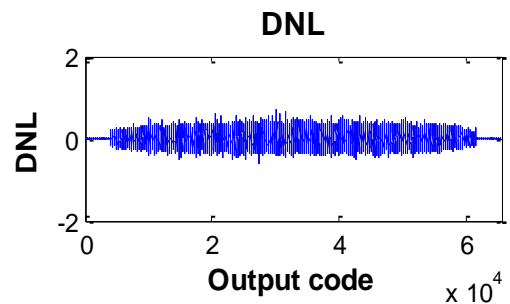
- 16-bit ADC with $f_{\text{clock}}=80\text{MHz}$, $A_{\text{clock}}=1.5\text{V}_{\text{p-p}}$, $f_{\text{in}}=9.41\text{MHz}$, $A_{\text{in}}=3.03\text{V}_{\text{p-p}}$
 - ◆ Assume DNL lie in range $(\mu - Z_{\alpha/2}\sigma, \mu + Z_{\alpha/2}\sigma)$ with 95% probability

$$\text{DNL resolution, } \beta \geq \sqrt{\frac{Z_{\alpha/2}^2 \cdot \pi \cdot 2^{N-1}}{N_t}}$$

- ◆ The limitation of logic analyzer
 - The max. number of output data is 2^{20}
 - To get larger N_t , output data should be exported for many times
- ◆ $N_t=2^{20}$ ($\beta=0.614$ LSB)
- ◆ $N_t=2^{22}$ ($\beta=0.307$ LSB)



$(\text{DNL}^+, \text{DNL}^-) = (1.323, -0.92)$ (LSB)



$(\text{DNL}^+, \text{DNL}^-) = (0.698, -0.597)$ (LSB)

➔ Higher N_t would get more accuracy of static testing

Mismatch between A_{in} and A_{sin}

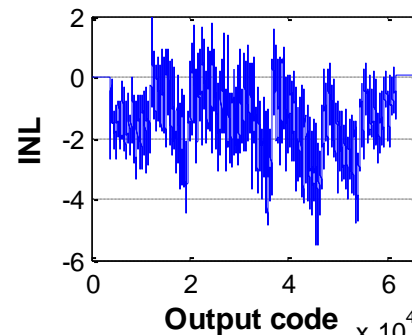
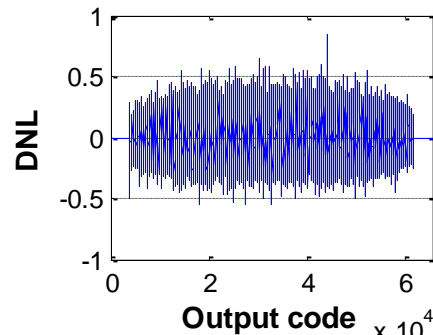
- A_{in} : actual signal amplitude generated from signal generator

A_{sin} : estimated amplitude for theoretical value in eq.(2)

- Using $v_i = -A_{sin} \cdot \cos(\pi \sum_{N_t} h(i) / N_t)$ to calculate DNL and INL

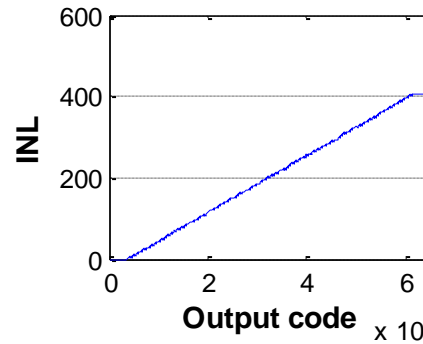
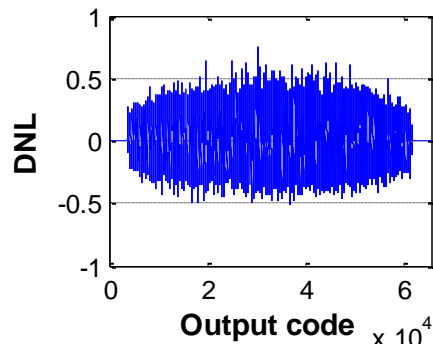
$A_{clock} = 1.65V_{p-p}$, $f_{clock} = 80MHz$, $A_{sin} = 1.50743V$, $f_{in} = 5MHz$, using K&L-5M-BPF

- ◆ A_{sin} matches to $A_{in} \Rightarrow A_{in} \approx A_{sin} = 1.50743 V$



DNL⁺ = 0.847 LSB
 DNL⁻ = -0.551 LSB
 INL(2¹⁶-1) = 0.09 LSB

- ◆ A_{sin} mismatches to $A_{in} \Rightarrow A_{in} = 1.497V \neq A_{sin}$



DNL⁺ = 0.756 LSB
 DNL⁻ = -0.504 LSB
 INL(2¹⁶-1) = 407 LSB

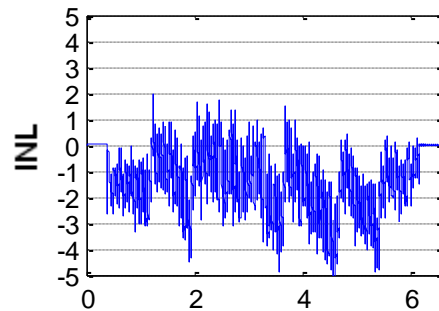
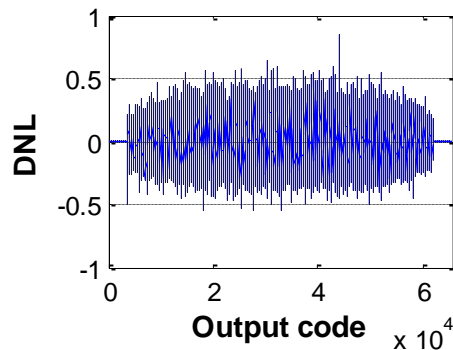
→ So A_{sin} must be equal to A_{in}

Mismatch between A_{in} and A_{sin} (Cont.)

- Using the method of calculating DNL and INL from P18~P19

$A_{clock}=1.65V_{p-p}$, $f_{clock}=80MHz$, $A_{sin}=1.50743V$, $f_{in}=5MHz$, using K&L-5M-BPF

◆ A_{sin} matches to $A_{in} \Rightarrow A_{in} \approx A_{sin} = 1.507425 V$

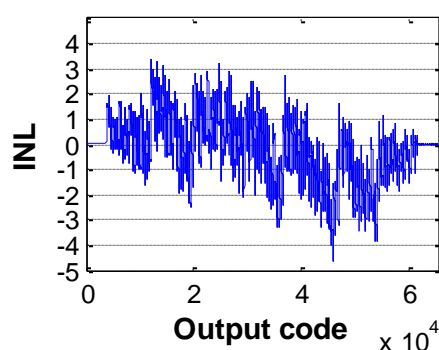
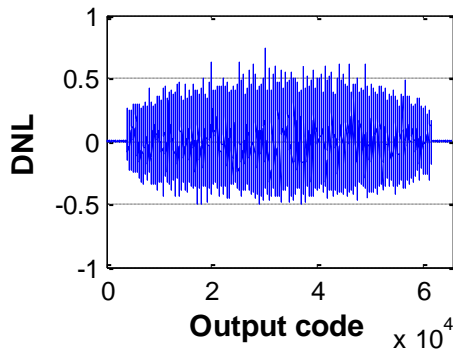


DNL⁺ = 0.847 LSB

DNL⁻ = -0.551 LSB

INL(2¹⁶-1) = 0 LSB

◆ A_{sin} mismatches to $A_{in} \Rightarrow A_{in} = 1.497V \neq A_{sin}$



DNL⁺ = 0.743 LSB

DNL⁻ = -0.507 LSB

INL(2¹⁶-1) = 0 LSB

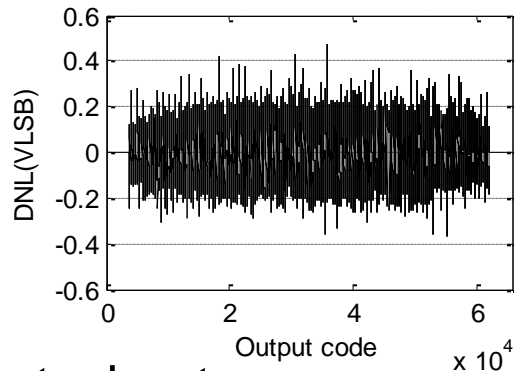
➔ Adopting this method, A_{sin} mustn't be equal to A_{in}

Comparison of Static Performance

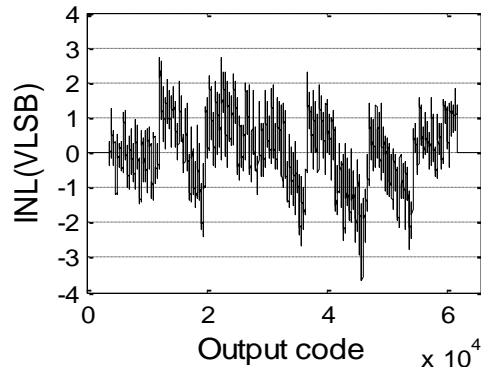
- Measured data

Conditions $\left\{ \begin{array}{l} A_{\text{clock}}=1.65V_{\text{p-p}}, f_{\text{clock}}=80\text{MHz}, A_{\text{in}}=3.03V_{\text{p-p}}, f_{\text{in}}=5\text{MHz} \\ \text{using 5M-BPF}, N_t=2^{24} \end{array} \right.$

- ◆ DNL



- ◆ INL

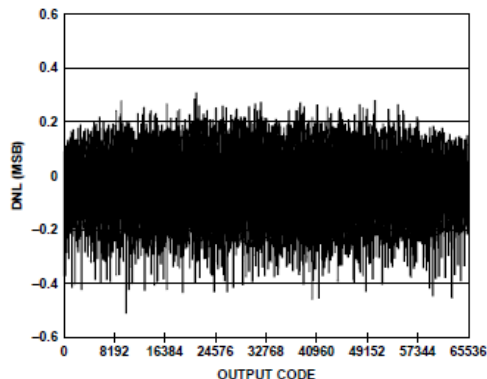


- ◆ Performance summary

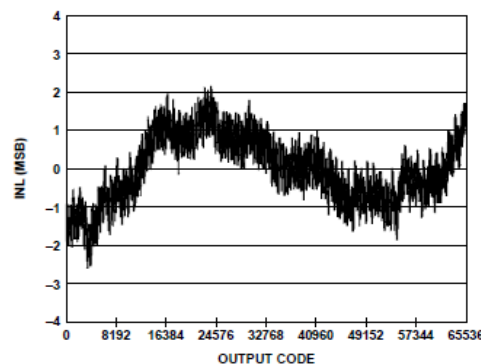
DNL⁺=0.471 LSB
 DNL⁻=-0.367 LSB
 INL⁺=2.6 LSB
 INL⁻=-3.62 LSB

- Datasheet

- ◆ DNL



- ◆ INL



- ◆ Performance summary

DNL⁺=0.3 LSB
 DNL⁻=-0.5 LSB
 INL⁺=2.1 LSB
 INL⁻=-2.5 LSB

Outline

- Introduction of ADC
- Static testing
- Dynamic testing
- Measurement example
- **Reference**

Reference

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- [8] Maxim Integrated, tutorial 748(2002, Jul 22). *The ABCs of ADCs: Understanding How ADC Errors Affect System Performance*
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